

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai)
UG - CSE, EEE & MECH Programs Accredited by NBA, New Delhi.
(An ISO 9001:2015 Certified Institution)
TRICHY - PUDUKKOTTAI ROAD, TIRUCHIRAPPALLI - 620 007.
Email: principalengg@miet.edu, contact@miet.edu
Website: - www.miet.edu



Ph: 0431 - 2660 303

# 1.2.2 Number of Add on /Certificate programs offered during the last five years (10)

	2019-2020				
Sl. No	Name of Add on /Certificate programs offered	Pg.No			
	EC19202 - Arduino Based Embedded System Design				
	Permission	2			
	Circular	3			
	Syllabus	4			
	Willing Student List	5-11			
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	Resource Person Details	14			
	Attendance	15-20			
	Question Paper	21-24			
	One Page Report Certificates	25 26-30			
	EC19201 - Hardware Modeling Using Verilog	20-30			
	Permission	32			
	Circular	33			
	Syllabus	34-35			
	Willing Student List	36-41			
2.	Course Delivery	42-43			
	Resource Person Details	44-45			
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Ph: 0431 - 2660 303

Date: 16.12.2019

To

The Principal

M.I.E.T Engineering College,

Trichy – 620007

Respected Madam,

Sub: Permission to conduct the certificate program – Reg...

We have planned to conduct the certificate program for our Second Year and Third year students from (3.1.2020 to 4.1.2020, 7.1.2020 to 11.1.2020, 13.1.2020, 20.1.2020 to 21.1.2020, 25.1.2020, and 27.1.2020 to 28.1.2020)

Name of the Certificate Program	Course Coordinator
Arduino based Embedded System Design	Mrs.G.Karthika AP/ECE

So kindly give us permission to conduct the course and to utilize the class room.

Thanking you

Course Coordinator

HOD/ECE

Principal



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CIRCULAR

Date: 18.12.2019

Sub: Certificate Program

It is planned to conduct the Certificate Program for the Second Year and Third year Electronics and Communication Engineering students.

The Certificate Program is short term certificate courses which are designed and offered by our department for the benefit of our students. Certificate Program will be conducted at free of cost and based on the performance of the participated students, the merit certificate will be issued after the successful completion of the course.

Students those who are willing to attend the below mentioned course can enroll their name to the course coordinator.

Name of the Certificate Program	Course Coordinator
Arduino_based Embedded System Design	Mrs.G.Karthika AP/ECE

Commencement of course from (3.1.2020 to 4.1.2020, 7.1.2020 to 11.1.2020, 13.1.2020, 20.1.2020 to 21.1.2020, 25.1.2020, and 27.1.2020 to 28.1.2020)

Time:4.45pm to 7.45pm

Course Coordinator

IQAC Coordinator

HODECE

Principal



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Website: - www.mlet.edu

Ph: 0431 - 2660 303

Course Program (II Year/IV Semester III Year/VI Semester)

Course Syllabus

Name of the course : ARDUINO based Embedded System Design

Course Code: EC19202

Course Coordinator: Mrs.G. Karthika AP/ECE

Total hours:38

Objectives:

Academic Year:2019-2020

- To provide knowledge of different Smart System applications.
- To familiarize students with Arduino as IDE, programming language & platform.
- To provide knowledge of Arduino boards and basic components.
- To develop skills to design and implement various smart system application.

Unit 1: Basics of Embedded System design

Introduction to embedded system, Components of Embedded System, Memory Organization, Advantages and Application of Embedded Systems, Real Time Embedded Systems.

Unit 2: Learning Arduino Platform

8

Introduction to Arduino, Pin configuration and architecture, Device and platform features (I/O Prts, Timers, Interrupts, Serial Port, ADC, etc.)

Unit 3: Arduino Programming

8

Introduction to Arduino IDE, Arduino data types, Variables and constants, Operators Control Statements, Arrays, Functions, Concepts of C language, Programming in Embedded- C.

Unit 4: Hardware Interfacing

LED's , Relays , Buzzer , Ultrasonic Sensors, Touch Sensors, Other different type of sensors and communication modules

Unit 5: Project Based on embedded system design using Arduino board.

7

Mini Project- Home Automation

Total Hours: 38

#### Course Outcomes:

- Familiar with Arduino environment and its applications.
- Able to understand Arduino programming
- · Able to Design Smart systems applications.
- Have a better understanding of essential problem solving and programming concepts.
- Apply programming knowledge and skills to design and implement reliable software systems that take into account software assurance concepts.

#### Books / Reference material required:

- 1. Arduino-Based Embedded Systems: By Rajesh Singh, Anita Gehlot, Bhupendra Singh, and Sushabhan Choudhury.
- 2. https://www.arduino.cc/en/Tutorial/HomePage
- Arduino Made Simple by Ashwin Pajankar
- 4. Embedded C, Pont, Michael J
- 5. ARM System Developer's Guide Designing and Optimizing System Software by: Andrew N Sloss, Dominic Symes, Chris Wright; 2004, Elsciver
- 6. ARM System On Chip Architecture, Furber, Steve

7. Assembly Language Programming: ARM Cortex - M3: Mahout, Vincent

Course Coordinator



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#### Willing Student list

CP1 Coordinator: Mrs.N.Latha AP/ECE and Dr.A Suresh Kumar Ap/ECE

CP2 Coordinator: G.Karthika AP /ECE

Academic Year: 2019-2020

SL. NO	STUDENT NAME	CP1 Hardware Modeling	CP2 Arduino based
		Using Verilog	Embedded System Design
1.	Abdul Hameed.A.H		√.
2.	Amirtha Varshini. M		<b>√</b>
3.	Bharathi. M		1
4.	Christina Jeny. S		<b>✓</b>
5.	Dhivya. R		<b>√</b>
6.	Fazil Ahamed. M		<b>✓</b>
7.	Jeevabharathi. M		<b>√</b>
8.	Kavimitha. S		<b>V</b>
9.	Lalith, R		<b>√</b>
10.	Manisha Christy. J		1
11.	Manju. K	, v	<b>√</b>
12.	Mohamed Arshath Ibrahim. S		<b>√</b>
13.	Mohamed Hisham. M		1
14.	Mohamed Rifai. H		✓
15.	Mohamed Riyaz. A		✓

SL. NO	STUDENT NAME	CP1 Hardware Modeling Using Verilog	<u>CP2</u> Arduino based Embedded System Design
_16.	Neeraja. K		·
17.	Prethiv Bharathi. C		<b>✓</b>
18.	Ramya. B		✓
19.	Riyaz Sait. A		<i></i>
20.	Sagulhammed. D		✓ .
21.	Sathya, M		<b>✓</b>
22.	Sneha. P		<b>√</b>
23.	Suruthi, B		<b>√</b>
24.	Thamar Mohamed		✓
25.	Thasneem. MI		<b>→</b>
26.	Vasimakaram. A		✓
27.	Vineeth Kumar. R	-	
28.	Vishnupriyan. R		<b>√</b>
29.	Vijay. K		
30.	Aabitha Begam. S	<b>✓</b>	£
31.	Abdul Ajeez. A	V	
32.	Abdul Rahman. M	<b>-</b>	name of the same o
33.	Afsana. A	91	
34.	Ahamed Aakif. Z		
35.	Akash, S		
36.	Akshaya. M		

SL. NO	. STUDENT NAME	CP1 Hardware Modeling Using Verilog	<u>CP2</u> Arduino based Embedded System Design
37.	Ammu, P		
38.	Ammu. S		
39.	Annal Jebaseeli D	✓	
40.	Antony Jero. J	<b>✓</b>	
41.	Arthi. J	<b>✓</b>	4
42.	Asrath Nisha. S		
43.	Boomika. P		✓
44.	Chaandhini, C	V	T
45.	Daniel Vinith. G	V	
46.	Defi Christina, C	*	✓
47	Deiva Rani. M		<b>√</b>
48.	Fazil Mohammed. B		<b>✓</b>
49.	Gayathri. K		<b>✓</b>
50.	Harini. P		
51.	Hasiba Banu. H	✓ ·	
52.	Hina. M	<b>√</b>	
53.	Janani. M	<b>/</b>	
54.	Jansirani. K	✓	
.55.	Jasmine, E	<i>J</i>	F
56.	Karan. M		✓
57.	Kavitha. M	V	

SL. NO	STUDENT NAME	CP1 Hardware Modeling Using Verilog	CP2 Arduino based Embedded System Design
58.	Kowsalya, K		Deargn
59.	Krishnapriya. K		
60.	Manikandan. T		
61.	Mathina Beevi. S	✓ ×	
62.	Mohamed Rizvanudeen. M	.	✓.
63.	Mohamed Suwaidee. M		<b>√</b>
64.	Mohamed Ibrahim. M		1
65.	Niranjani. B		
66.	Nithiksha. N		*
67.	Nithish Kumar. S		
68.	Pavithra. C	<b>-</b>	
69.	Puvanithy. M	✓.	
70.	Rizvana Begam, T	/	
71.	Sabarinath, C		
72.	Sabitha. S		))
73.	Safa Almaz. MS	<b>/</b>	
74.	Sathiya Sheela. S	<b>→</b>	
75.	Selciya. M		
76.	Shakthivel. A	V	*
77.	Shalini, B		✓
78.	Suruthi. M		<b>√</b>

SL. NO	. STUDENT NAME	CP1 Hardware Modeling Using Verilog	<u>CP2</u> - Arduino based Embedded System
79.	Tamil Mani. B	1251	Design
80.	Thajudeen. T		
81.	Thilsara. S	_	
82.	Vengatesh Kumar. M		✓
83.	Vigneshwaran. M	✓.	
84.	Vimal Athithan. M		
85.	Yogapriya. S		
86.	Zam Zam Haliya. A	1	
87.	Nisha Shalini. K	· ·	
88.	Deepa. A		
89.	Hari Vijay. R		
90.	Kiruthigha. K		✓.
91.	Monica. J		√
92.	Vetriselvi, A		<b>√</b>
93.	Aarthi. N	<b>~</b>	
94.	Abarna, N		
95.	Abdul Malik. T		
96.	Ameer Sultan. J		
97.	Ashik Mohamed. A		
98.	Asrin Jaswani. S	<b>*</b>	
99.	Bhuvaneswari. S		

SL. NO	STUDENT NAME	Hardware Modeling Using Verilog	<u>CP2</u> Arduino based Embedded System Design
100.	Gayathri Vani. A	· V	•
101.	Guna Sunthari. B	_ /	
102.	Hari Haran. R		
103.	Lavanya. P	· /	
104.	Madhumitha. C		
105.	Mohamed-Faisal, S		
106.	Mohamed Imran. M	V	
107.	Mohamed Rafik, M	<b>√</b>	
108.	Mohamed Riaz. A	V .	
109.	Mohamed Rizwan, B		
110.	Mohamed Sirajudeen. S		
111.	Muhammed Azarudeen. J		
112.	Muthulakshmi. M	<b>√</b>	
113.	Muthulakshmi, S	V	
114.	Pavithra Devi. P	<b>*</b>	
115.	Pearly, J	<b>√</b>	-
116.	Racisa. A	V	
117.	Rifansiya. S	<b>√</b>	
118.	Shabhan, R	V	
119.	Souban Mohamed. S		2
120.	Suguna. S	V	

SL. NO	STUDENT NAME	CP1 Hardware Modeling Using Verilog	CP2 Arduino based Embedded System Design
= <sub>121</sub> .	Surendhar, B		-Design
122.	Syed Sadham. N	-	
123.	Thaslima Afrin. S	- /	
124.	Vishnu Priya. N.J	- V	
125.	Viveka. K	· ·	
126.	Fayaz Ahamed. A	<b>√</b>	
127.	Haribaskar. S	V	
128.	Janani. R	<b>√</b>	
129.	Mohamed Ishan. M	<b>/</b>	
·130.	Mohamed Rayan. A.S		
131.	Mohana Sundari. P		
132.	Vishnuvarthan. N		

Course Coordinator

HORAE CE

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### Certificate Program (II Year /IV Semester and III Year/VI Semester)

Program Schedule

Name of the Course: Arduino based Embedded System Design

Course Code: EC19202

Course Coordinator: Mrs.G.Karthika AP/ECE

Total Hours: 38

Academic Year: 2019-2020

Sl.No	Topics to be Covered	Hours	Date of Delivery
1.	Introduction to embedded system	1	
2.	Basics of Embedded System design	2	3.1.2020
3.	Overview of basic electronics and digital electronics	3.	
4.	Introduction to Microcontroller	4	
5.	Introduction to Microprocessor	5.	4.1.2020
6.	Memory Organization	6	-A11
7.	Advantages and Application of Embedded Systems	7	
8.	Real Time Embedded Systems	8	7.1.2020
9.	Learning Arduino Platform	9	
10.	Introduction to Arduino	10	
11.	Pin configuration and architecture	11	8.1.2020
12.	Device and platform features	12	
13.	Concept of digital and analog ports	13	
14.	I/O Prts, Timers	14	9.1.2020
15.	Interrupts, Serial Port	15	
16.	ADC	16	
17.	Arduino Programming	17	10.1.2020
18.	Introduction to Arduino IDE	18	
19.	Arduino data types	19	
20.	Variables and constants	20	11.1.2020
21.	Operators Control Statements,	21	

Sl.No	Topics to be Covered	Hours	Date of Delivery
22.	Arrays, Functions	22	
23	Concepts of C language,	23	13.1.2020
24.	Arduino i/o Function	24	
25.	Programming in Embedded- C.	25	
26.	Hardware Interfacing- LED's , Relays Buzzer	26	
27.	Other different type of sensors and communication modules	27	20.1.2020
28.	Temperature sensor	28	
29.	Water Detector/sensor	29	21.1.2020
30.	Ultrasonic Sensors	30_	
31.	Touch Sensors,	31	
32.	Arudino Communication	32	25.1.2020
33.	Parallel Communication	33	
34.	Serial Communication Modules	34	
35.	Types of serial Communication	35	27.1.2020
36.	Arduino UART	36	
37.	GSM Arduino Interfacing	37	28.1.2020
38.	GPRS Arduino Interfacing	38	28.1.2020

Course Coordinator

HoD/ECE

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### Resource Person Details

Title of the program	Arduino_based Embedded System Design
Course Code	EC19202
Duration and timing of the program	38 Hrs, 09.00 AM – 05.30 PM
Name of the resource person	Mrs.G.Karthika AP/ECE
Photo of the resource person	
Email address	Karthika.g@miet.edu
Contact number	9865197766
Designation	Assistant Professor
Educational qualification	<ul> <li>B.E -Electronics and Communication Engineering 2006 in Sudharsan Engineering College affiliated to Anna University Chennai with CGPA 70%.</li> <li>M.E -VLSI DESIGN (2011-2013) in M.I.E.T Engineering College, affiliated to Anna University Chennai with CGPA 8.5.</li> </ul>
Experience	➤ Teaching Experience – 10 Years.



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# Certificate Course (II Year/ IV Semester, III Year/VI Semester) Attendance Sheet

Name of the course: Arduino based Embedded System Design

Course code: EC19202

Course coordinator: Mrs.G.Karthika AP/ECE

Academic Year: 2019-2020

	Tear. 2017-	1				T -		1		-		_			177							
SL.NO	ROLL NO	STUDENT NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	18	2
	E1184001	Abdul Hameed.A.H	1	1	a	1	a	,	1	,	a	a	1	1	,	a	a	,	١,	,	OL	6
2.	E1184002	Amirtha Varshini, M	1	1	1	a	-	1	1	1	_	1	1	,	,	1	,	,	·,	1	1	-
3.	E1184003	Bharathi. M	1	a	1	1	1	a	a	1	2	1	,	a	1	,	a	/	a	,	2	
4.	E1184004	Christina Jeny. S	1	1	1	1	1	a	1	1	1	,		1	a	1	1	a		a	a	
5.	E1184005	Dhivya. R	1	,	a	1	1	a	1	,	a	a	a	1	,	1	1	a	-	a	1	/
6.	E1184006	Fazil Ahamed. M	a	a	1	a	a	a	1	,	,	1	1	,	a	1	a		,		-/	1
7.	E1184009	Jeevabharathi. M	a	1	,	a	1	a	1	1	,	,	<u></u>	,	/	-/	1	a	2	a		0
8.	E1184011	Kavimitha. S	1	,	,	1	,	1	a	1	,	a	a	,	1	1	1	1	,		a	-
9.	E1184012	Lalith. R	a	1	a	OL	-a	a	a	1	,	1	,	a	a	a	/	1	/	1	1	-
10.	E1184013	Manisha Christy. J	/	1	1	1	1	a	1	1	a	/	1	1	1	1	00	1	,	1	1	1
11.	E1184014	Manju. K	/	,	1	1.	1	A	/	à	1	a	1	1	1	1	1	1	/	/	1	1

PRINCIPAL
M.I.E.T. ENGINEERING COLLEGE
GUNDUR, TIRUCHIRAPPALLI-620 007.

1

SL.NO	ROLL NO	STUDENT NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	18	12
		State of Contract Contract (Contract Contract Co		10.7																	-	+
12.	E1184015	Mohamed Arshath Ibrahim. S	1	1	1	a	a	a	1	1	,	2	Q.	a	,	,	1	a	a	92	-	-
13.	E1184016	Mohamed Hisham. M	a	,	1	1	1	1	a	,	a		1	,	a	/	1	1	ci	1	1	G
14.	E1184017	Mohamed Rifai. H	1	,	1	a	a	a	/	a	1	,	a	1	0	1	a	1	1	1	1	1
15.	E1184018	Mohamed Riyaz. A	a	a	,	1	1	1	a	a	^	/	1	,	1	/	1	-	2	2		-
16.	E1184020	Neeraja. K	a	1	1	a	1	1	1	,	- a	,	,	,	1	1	1	9	1		a	1
17.	E1184021	Prethiv Bharathi. C	1	,	a	1	a	1	Or	,	1	1	/	a	1	/		1	_	-	1	1
18.	E1184023	Ramya. B	a	1	a	1	1	a		or	1	/	1	1	a	/.	/		a	4		1
19.	E1184024	Riyaz Sait. A	1	a	1	1	1	1	,	1	a	a	1	1	1	- (		/	/	1 a	-	
20.	E1184025	Sagulhammed. D	1	/	1	1	1	a	,	,	a	1	1	a	a	9	- /	1	1	2	-,	
21.	E1184026	Sathya. M	1	a	1	,		1	1	,	a	1	a	,	1	/	/	_	/	- 1	a	
22.	E1184027	Sneha, P	1	^	,	,		,	/	1	,	a	1	-	,	1	1	4	,		,	
23.	E1184028	Suruthi. B	1	,	a	1	/	a	a	,	,	1	a	,	,	a	Q.	,	,	-	/	-
24.	E1184029	Thamar Mohamed	0-	,	1	a	1	,	/	1	,	,	,		,	1	1	1		/	/	
25.	E1184030	Thasneem. ML	1	a	,	1	/	1	,	.,	a	$\frac{1}{1}$	<i>a</i>		1	/	1	7				_
26.	E1184031	Vasimakaram. A	1	4	1	a	a	/	1	,	1	/	1	0	a	a	1	/	2	+	/	-/
27.	E1184033	Vishnupriyan. R	a	,	1	a	1	1	,	1	/	,	/	,	1	/	1	1	a	,	,	_
28.	E1174018	Boomika. P	1	/	a	1	1	,	1	1	,	,	a	1	1	1	a	1	2	1		1
29.	E1174021	Defi Christina. C	1	/	a	,	1	,	/	1	,	į		0	/	1	/	7	1	0	a	8

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SL.NO	ROLL NO	STUDENT NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	18	2
30.	E1174022	Deiva Rani. M	1	1	1	a	1	a	a	1	1	1	,	a	1	a	1	a	١,		<del>  .</del>	-
31.	E1174023	Fazil Mohammed. B	a	1	1	1	a		1	1	0	1	a	,	a	a	1	1	,	a	/	1
32.	E1174024	Gayathri. K	1	a	1	a	1	1	0	,	a	1	a	a	1	1	a	1	1	a.	1	1
33.	E1174032	Karan. M	1	1	1	a	1	1	1	,	1	a	1	1	a	1	a	1	1,		_/_	-
34.	E1174039	Mohamed Rizvanudeen. M	,	1	1	,	,	a	1	,	1	1	1	2	1	a	-	a	1	a	1	1
35.	E1174040	Mohamed Suwaidee. M	a	1	1	a	1	1	1	a	1	1	1	/	,	/	j	1	or	1	1	-
36.	E1174041	Mohamed Ibrahim. M	1	1	1	1	1	,	1	a	1	1	1	a	1	æ	/	1	1	a	/	/
37.	E1174056	Shalini. B	1	2	1	1	1	1	1	1	a	1	,	,	1,	,		a	1	-	,	_/
38.	E1174057	Suruthi. M	1	1	1	,	1	1	1	,	a	1	1	a	a	-	a	1	1	1	a	
39.	E1174062	Vengatesh Kumar. M	a	1	1	,	a	,	1	a	1	1	1	a	a	9	ai	,	,	1	Ci	1
40.	E2184070	Kiruthigha. K	1	1	1	0	1		1	/	1	7	a	1	/	,	,	1	1	/	a	(
41.	E2184072	Monica. J	a	1	1	1	1	1	a	a	1	,	a	a	1	a	1	a	/	1	,	1
42.	E2184074	Vetriselvi. A	1	ex	1	,	1	/	1	1	1	1	,	a	1	a	1	a	7	1	,	1
		Total No Students Presents	26	28	31	25	24	21	19	21	26	28	31	-	27	111111	2.9	22	31	32	31	20
		Total No Students Absent	16	14		12	18	21	20	21	16	14			11000	1	/10 Mod	20	11	10	11/	7
		Signature Course Coordinator	P	P	P	P	P	(A)	B	P	P			10)	and /	P	(P)	P	P	P	P	厂厂

SL.NO	ROLL NO	STUDENT NAME	21	22	23	24	25	26	27	28	29	30	31	32	33	34	.35	36	37	38	39	40	41	42
									,							/*								
1.	E1184001	Abdul Hameed.A.H	- 1	1	a	1	1	1	1	a	1	1	a	1	1	1	a	1	1	1	a	,	,	0
2.	E1184002	Amirtha Varshini. M	a	1	1	,	1	1	a	1	,	1	1	1	1	a	1	a	a	.,	1	a	,	
. 3.	E1184003	Bharathi. M	,	,	a	1	a	a	1	,	1	a	1	1	1	1	1	1	,	1	a	1	1	1
4.	E1184004	Christina Jeny. S	1	a	a	a	,	1	1	1	,	1	1	1	a	1	,	-	,	/	a	,	/	1
5,	E1184005	Dhivya. R	a	1	1	1	,	1	,	1	a	1	a	1	1	1	0	1	./	0	,	a	1	1
6.	E1184006	Fazil Ahamed. M	1	1	a	,	1	a	,	,	1	a	1	a	1	,	a	a	,	a	/	,		a
7.	E1184009	Jeevabharathi. M	1,	,	Oc	1	,	1	1	1	1	1	1	a	,	a	1	1	a	1	/	,	1	
8.	E1184011	Kavimitha. S	a	,	,	a	a	1	a	1	a	1	,	,	/	4	/	a	1	1	4	/	,	
9.	E1184012	Lalith. R	a	1	1	1	1	1	a	1	-,	1	_	,	/	v,	_		1841	1	a	/	,	_
10.	E1184013	Manisha Christy. J	1	a	1	a	1	1	,	0_	-/	/	^	/	0		a	1	/	/	a	1	1	_
11.	E1184014	Manju. K	a	1	0	,	1	a	0	1	1	,	2	/		_/		·a	/	/	1	a	4	
		Mohamed Arshath	1		0	-/		$\neg$	-	-			-	1		1	/	-		-	(	a	/	/
12.	E1184015	Ibrahim. S	1	a	1	0-	1	1	1	1	a	1	1	a	1	1	a	1	1	1	1	a	1	1
13.	E1184016	Mohamed Hisham. M	a	1	1	,	a	,	/	a	1	1	a	,	a	/	1		a	1	a	/	1	,
14.	E1184017	Mohamed Rifai. H	a	1	1	1	a	1	a	1	,	1	1	/	6	1	1	a	1	,	a	a	1	1
15.	E1184018	Mohamed Riyaz. A	1	1	1	,	1	1	1	1	1	/	1	,	1	,	1	a	,	1	/	,	7	/_

SL.NO	ROLL NO	STUDENT NAME	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
16.	E1184020	Neeraja. K	1	,	a	0	,	-,	,	2	a	1	a	,	,		,	,	,	,	ļ,		_	
17.	E1184021	Prethiv Bharathi. C	1	a	1	,	1	,	1	1	1	1	1	a	a	a	1	a	a	1	1	0	1	0
18.	E1184023	Ramya. B	a	1	a	1	a	1	a	a	a	1	1	1	1	a	1	a	1	a	1	1	-	
19.	E1184024	Riyaz Sait. A	1	1	1	a		,	1	,	1	a	,	1	0	a	1	,	,	1	1	a	. /	0
20.	E1184025	Sagulhammed. D	1	a	1	a	-	a	,	,	1	1	a	1	1	1	1	a	a	0	,	a		1
21.	E1184026	Sathya. M	,	1	1	a		,	1	,	1	1	a	1	,	1	a	1	1	1	,	1	_/ a	On 1
22.	E1184027	Sneha. P	a	a	a	/	1	1	1	1	a	a	1	1	1	1	a	1	a	.,	a	a	1	1
23.	E1184028	Suruthi. B	,	1	1	1	1	1	a	1	1	,	1	a	a	a	1	,	1	ia	1	,		
24.	E1184029	Thamar Mohamed	1	1	1	1	a	1	,	1	/	1	a	,	a	,	a	7	a	1	a	1	a	1
25.	E1184030	Thasneem. ML	1	1	Oc	1	,	a	-/	a	0	1	a	-/-	1	1	,	0	,	,	1	a	-	a
26.	E1184031	Vasimakaram. A	a	a	1	a	1	/	1	,	,	,	/	,	,	1	a		a'	1	,	1	a	a.
27.	E1184033	Vishnupriyan. R	1	1	1	1	1	1	,	1	^	,	/	1	,	a	1	,	1	,	,	,	CA	_/ Q
28.	E1174018	Boomika. P	a	1	1	1	a	,	1	1	a	1	a	1	,	,	a	1	,	,	a	1	1	a
29.	E1174021	Defi Christina. C	1	a	1	-/	/	1	a	1	1	1	,	1	a	1	1	1	a	,	1	1	a	1
30.	E1174022	Deiva Rani. M	1	1	1	,	1	1	1	1	1	1	a	1	a	1	a	/	/	à	,	a	,	a
31.	E1174023	Fazil Mohammed. B	a	a	/	,	a	1	1	,	a	1	/	1	1	O.	1	a	a	,	a	/	,	0
32.	E1174024	Gayathri. K	1	1	a	,	1	,	1	,	1	1	a	1	,	0	a	1	1	/	1	1	,	0
33.	E1174032	Karan. M	1	1	a	,	^	,	a	1	1	1	,	1	a	1	1	a	a	a	1.0	20 /	,	a

		amvin mvm vi v v n	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37.	38	39	40	41	42
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34.	E1174039	Mohamed Rizvanudeen. M	1	1	1	/	1	1	1	)	1	1	1	/	1	(	1	1	1	1	1	1	1	1
35.	E1174040	Mohamed Suwaidee. M	7	5	1	1	1	- 5	1	1	1	1	1	/	1	1	,	,	1	1	1	-	1	1
36.	E1174041	Mohamed Ibrahim. M	1	1	1	1	1	1	1	1	1	J	1	-/	ſ	1	. /	1	1	1	1	1	1	1
37.	E1174056	Shalini. B	1	7	1	1	1	1	(	1	1	1	1	1	ſ	1	1	1	1	1	1	1	1	1
38.	E1174057	Suruthi. M	,	1	1	1	1	ſ	1	(	/	1	1	1	1	1	1	1	1	1	1	1	1	1
39.	E1174062	Vengatesh Kumar. M	1	1	1	1	1	f	1	1	1	1	1	J	1	/	1	1	/	1	1	1	1	1
40	E2184070	Kiruthigha. K	1	1	1	1	1	/	,	1.	/	1	1	,	1	1	1	1	1	1	/	1	1	1
41.	E2184072	Monica. J	/	J	/	1	1	1	(	/	/	1	/	1	1	1	/	,	1	r	1	1	1	1
42.	E2184074	Vetriselvi. A	1	1	1	1	1	,	1	1	1	1	/	1	1	1	1:	1	1	1	1	1	1	1
	Т	otal No Students Presents	33	30	29	32_	3	33	30	31	23	30	33	30	30	30	29	32:	31	33	30	33	31	32
		Total No Students Absent	C	12	13	w	tt	9	12	11	7	12-	9	12	12	12	13	20	1 1	9	12	e <sub>]</sub>	k	30
8	Sign	nture Course Coordinator	10	P	P	(P	P	P	®	(E)	0	0	æ_	æ	0	@	C	C.	0	do-	P	æ	(Jo	(B)

Course Coordinator

HoD/ECE

PRINCIPAL M.I.E.T. ENGINEERING COLLEGE GUNDUR, TIRUCHIRAPPALLI-620 007.

Principal

6



(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai)
UG - CSE, EEE & MECH Programs Accredited by NBA, New Delhi,
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'Website: - www.miet.edu

Ph: 0433

Ph: 0431 - 2660 303

#### Certificate Program Assessment Test

Name of the course: Arduino based Embedded System Design Course Code: EC19202

Academic Year: 2019-2020

Date:14.12.2019 Time: 01:30 hrs

- 1. Which design allows the reuse of the software and the hardware components?
  - a. Memory Design
  - b. Input design
  - c. Platform-based design
  - d. Peripheral design
- 2. Which design considers both the hardware and software during the embedded design?
  - a. Memory Design
  - b. Software/ hardware co design
  - c. Platform-based design
  - d. Peripheral design
- 3. What does API stand for?
  - a. Application Programming Interface
  - b. Address Programming Interface
  - c. Accessing peripheral through the interface
  - d. None of them
- 4. Which design activity can be used for the mapping operation to hardware?
  - a. High-level transformation
  - b. Scheduling
  - c. Compilation
  - d. Hardware / Software partitioning

	6. Which of the following tarithmetic?	ool can replace floa	ting-point arithmetic with fixed-point
	a. FAT		2
	b. SDS		
	c. FRIDGE		
	d. VFAT		
58	7. Which of the following can	reduce the loop overhe	ead and thus increase the speed?
	a. loop tiling		
	b. Loop unrolling		
	c. loop fusion		
	d. loop permutation		* ×
	8. How many types of arduino of	do we have?	
	a) 5		
	b) 6		
	c) 8		
	d) 6		
	9. What is the microcontroller u	ised in Arduino UNO?	?
	a) ATmega328p		
31	b) ATmega2560		
	c) ATmega32114		
	d) AT91SAM3x8E		
	10. What does p refer to in ATn	nega328p?	
	a) Production		
			7
		8	M. L.
			M.I.E.T. ENGINEERING COLLEGE
		Page 22 of 62	GUNDUR, TIRUCHIRAPPALLI-620 007.

5. Which process can be used in analyzing the set of possible designs?

a. Scheduling

d. Compilation

b. Design space exploration

c. Hardware / Software partitioning

b) Pico-Power			
c) Power-Pico			
d) Programmable on chip			
11. Arduino shields are also called as _		40	
a) Extra peripherals			
b) Add on modules	•	-	
c) Connectivity modules		1921 III., 192	
d) Another Arduinos			
		¥.	
12. What is the default bootloader of the	e Arduino UNO	)?	
a) Optiboot bootloader			
b) AIR-boot			1
c) Bare box			
d) GAG			1
<ul><li>13. Does the level shifter converts the voltransistor logic.</li><li>a) True</li><li>b) False</li></ul>			i dansistor-
<ul><li>14. Which is the software or a programn</li><li>a) Assembly Language</li></ul>	ning language u	sed for controllin	g of Arduino?
b) C Languages			
c) JAVA			
d) Any Language			
15. Do Arduino provides IDE Environme	ent?		
a) True	ciic.		
b) False	E		
16. A program written with the IDE for A	Arduino is calle	d	
a) IDE source		market mark & MARIETTA	
b) Sketch			

c) Cryptography
d) Source code
17. How many digital pins are there on the UNO board?
a) 14
b) 12
c) 16
d) 20
18board allows sewn into clothing.
a) UNO
b) RedBoard
e) LilyPad
d) Mega
19. How many analog pins are used in Arduino Mega board?
a) 16
b) 14
c) 12
d) 8
20. Which of the following is a process of analyzing the set of possible designs?
a) design space exploration
b) scheduling
c) compilation
d) hardware/software partitioning
21. Which of the following is a meet-in-the-middle approach?
a) peripheral based design
b) platform based design
c) memory based design
d) processor design



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Ph: 0434 2000 200

Report

Name of the course: Arduino based Embedded System Design

Course Code: EC19202

Course Coordinator; Mrs.G.Karthika AP/ECE

Total Hours: 36

Academic Year: 2019-2020

I hereby affirm that the entire course contents listed in the course syllabus of the certificate program "Arduino based Embedded System Design" have educated to the students as the part of the prescribed co – curricular activities through Certificate Program.

They have been given liands on session on the topics mentioned and students clearly understood the hardware configuration of the system.

The certificate program titled as "Arduino based Embedded System Design" has been conducted in the beginning of the semester and course delivery along with attendance of the students was recorded.

All the students were actively attended this certificate Program and performed well throughout the program and eligible students received the certificate.

Course Coordinator

HoD/ECE

Principal

	Randa Andrew
7	MILET ENGINEERING COLLEGE STATE
	Trichy, Pudukkottai Road, Trichy - 620 007.
	Course Completion Certificate
	INSTITUTIONS Since 1984
	This is to Certify that Mr/Ms. p. Sneha
9 6	of The Fire has Completed the Course on
	Arduino Rased Embedded System Design from 3.1.2020 to 28.1-2020
- 19	
	Course Coordinator  MILE.T. ENGINEERING COLLEGE  Principal
Y: V	M.I.E.T. ENGINEERING COLLEGE GUNDUR, TIRUCHIRAPPALLI-620 007.
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	M.I.E.T. ENGINEERING COLLEGE Trichy, Pudukkottai Road, Trichy - 620 007.
	Course Completion Certificate INSTITUTIONS  Course Completion Certificate
	Since 1984
	This is to Certify that Mr/Ms. R Vishou Diyan
	of TI FCE has Completed the Course on
	Arduino Based Embedded syelem from 31-2020 to 28.1.2020 Design
	2. Ahr - K get alt alt
	Course Coordinator  M.E.T. ENGINEERING COLLEGE GUNDUR, TIRUCHIRAPPALLI-620 007.

	EN ROSE AND
	REP MIET ENGINEERING COLLEGE STY
	Trichy, Pudukkottai Road, Trichy - 620 007.
eri <b>d</b> ik	Course Completion Certificate
	INSTITUTIONS Since 1984
	This is a Contifue that Mar/Mar P Property Alice
	This is to Certify that Mr/Ms. B. Fazil Ahamed  of III FIE has Completed the Course on
	Arduing Based Embedded system from 3.1.2020 to 28.1.2020
	Design
	Course Coordinator And Principal
	PRINCIPAL M.I.E.T. ENGINEERING COLLEGE GUNDUR, THRUCHTBAPPALLI-620 007.

	ENSTERNS FERS FERS FERS FERS FERS FERS FERS FER
	MILE.T. ENGINEERING COLLEGE STOPE
104	Trichy, Pudukkottai Road, Trichy - 620 007.
	Course Completion Certificate INSTITUTIONS Course Completion Certificate
	Since 1984
	This is to Certify that Mr/Ms. R. Shalini
	of (i) I= (E) has Completed the Course on
	Arduinphaeed Embedded system from 3-1.2020 to 28.1.2020 Design
	Design
	Course Coordinator Hod Auly Principal
	Course Coordinator  PRINCIPAL  PRINCIPAL  MI.E.T. ENGINEERING COLLEGE  MI.E.T. ENGINEERING COLLEGE  CHABUR TRUCHBAPPALL 620 007.

	MILET ENGINEERING COLLEGE Trichy, Pudukkottai Road, Trichy - 620 007.
	Course Completion Certificate
74.	Since 1984
	This is to Certify that Mr/Ms. C. Deli Chnstina
	of 111 ECE has Completed the Course on  Arduing Based Embedded system from 3.1.2020 to 281.2020  Design
	Course Coordinator Hou Aug Principal (A)
	PRINCIPAL M.I.E.T. ENGINEERING COLLEGE GUNDUR, TIRUCHIRAPPALLI-620 007.

22. Which design activity is in charge of mapping operations to hardware? a) scheduling . b) high-level transformation c) hardware/software partitioning d) compilation 23. In which design activity, the loops are interchangeable? a) compilation b) scheduling c) high-level transformation d) hardware/software partitioning 24. Which activity is concerned with identifying the task at the final embedded systems? a) high-level transformation b) compilation c) scheduling d) task-level concurrency management 25. Which of the following device can transfer the vector table from the EPROM? a) ROM b) RAM c) CPU d) peripheral

Course Coordinator

HoD/ECE

Principal



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Website: - www.mlet.edu

Ph: 0431 - 2660 303

Date: 20.05.2019

To

The Principal

M.I.E.T Engineering College,

Trichy - 620007

Respected Madam,

Sub: Permission to conduct the certificate program – Reg...

We have planned to conduct the certificate program for our Third and Final year students from 23.05.2019 to 30.05.2019)

Name of the Certificate Program	Course Coordinator	
Hardware Modeling Using Verilog	Mrs.N.Latha AP/ECE and Dr.A Suresh Kumar Ap/ECE	

So kindly give us permission to conduct the course and to utilize the class room.

Thanking you

Course Coordinator

HoD/ECE

Principal



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Website: - www.miet.edu

Ph: 0431 - 2660 303

21.05.2019

#### CIRCULAR

Sub: Certificate Program

It is planned to conduct the Certificate Program for the Third and Final year Electronics and Communication Engineering students.

The Certificate Program are short term certificate courses which are designed and offered by our department for the benefit of our students. Certificate Program will be conducted at free of cost and based on the performance of the participated students, the merit certificate will be issued after the successful completion of the course.

Students those who are willing to attend the below mentioned course can enroll their name to the course coordinator.

Name of the Certificate Program	Course Coordinator		
Hardware Modeling Using Verilog	Mrs.N.Latha AP/ECE and Dr.A Suresh Kumar Ap/ECE		
	Course from 23.05.19 to 30.05.19 09.30 AM - 05.00 PM		

Course Coordinator

IOAC Coordinator

HoD/ECE

Principal=



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Website: - www.mlet.edu

Ph: 0431 - 2660 303

### Certificate Program (III Year /V semester and IV Year/VII Semester)

Course Syllabus

Name of the course: Hardware Modeling Using Verilog

Course Code: EC19201

Course Coordinator: Mrs.N.Latha AP/ECE and Dr.A Suresh Kumar AP/ECE

Total hours: 36

Objectives:

Academic Year: 2019-2020

- Designing digital circuits, behavioral and RTL modeling of digital circuits using Verilog HDL.
- Verifying these models and synthesizing RTL models to standard cell libraries and FPGAs.
- Students gain practical experience by designing, modeling, implementing and verifying several digital circuits.
- This course aims to provide students with the understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using provided software tools.
- Design digital components and circuits that are testable, reusable and synthesizable.

#### Unit 1: Overview of Digital Design

8

Principles of combinational logic, Combinational circuit design-Combinational Functions, Analysis and design of combinational logic. Sequential Logic Circuits-Latches and Flip-Flops, Counters and FSM design and their applications

#### Unit 2: Basic Concepts of Verilog

7

Introduction to Verilog - modules and module instances, parts of a simulation, design block, stimulus block, trends in HDLs. Basic Concepts- Verilog HDL. Hierarchical Modeling Concepts-Top-down and bottom-up design methodology. Language and conventions: Identifier, data types, system tasks, compiler directives.

#### Unit 3: Gate-Level Modeling

7

Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delay and instantiation. **Dataflow Modeling** Continuous assignments, delay specification, expressions, operators, operator types.

#### Unit 4: Behavioral modeling

7

Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multi way branching, loops, sequential and parallel blocks.

Unit 5: Application

7

Simulation/implementation exercises of combinational, sequential and DSP kernels on Xilinx/Altera boards

Total Hours: 36

#### Course Outcomes:

- Understand a digital circuit of a system. .
- > Explain syntax, lexical conventions, data types, modules and ports.
- Model the digital system using gate level and dataflow description.
- Model the digital system using behavioral description.
- > Analyze the steps involved in synthesis of HDL code
- >-Implement a hardware using FPGA

Books / Reference material required:

- Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition, Samir Palnitkar, 2003, Prentice-Hall, Inc.
- -2. Digital Logic Applications and Design by John M Yarbrough, Thomson Learning, 2001

Course Coordinator

IOAC Coordinator

HoD/ECE

Principal



Ph: 0431 - 2660 303

### Willing Student list

CP1 Coordinator: Mrs.N.Latha AP/ECE and Dr.A Suresh Kumar Ap/ECE

CP2 Coordinator: G.Karthika AP /ECE

Academic Year: 2019-2020

			apulier.
SL. NO	STUDENT NAME	CPI Hardware Modeling Using Verilog	CP2 Arduino based Embedded System Design
1.	Abdul Hameed.A.H		✓ ✓
2.	Amirtha Varshini. M		<i>'</i>
3.	Bharathi. M	1	<b>√</b>
4.	Christina Jeny. S		<b>√</b>
5.	Dhivya. R		V.
6.	Fazil Ahamed, M		<b>V</b>
7.	Jeevabharathi. M		<b>✓</b>
8.	Kavimitha. S		· · · · · · · · · · · · · · · · · · ·
9.	Lalith. R		. ✓
10.	Manisha Christy. J		✓
11.	Manju. K		<b>√</b>
12.	Mohamed Arshath Ibrahim. S		<b>√</b>
13.	Mohamed Hisham. M		<b>V</b>
14.	Mohamed Rifai. H		✓
15.	Mohamed Riyaz. A		<b>√</b>
16.	Neeraja. K		✓ 8
17.	Prethiv Bharathi. C		1
18.	Ramya. B		✓ ·

SL. NO	STUDENT NAME	CP1 Hardware Modeling Using Verilog	CP2 Arduino based Embedded System Design
19.	Riyaz Sait. A		✓ 1/2
20.	Sagulhammed. D		<b>√</b>
21.	Sathya. M		<b>√</b>
22.	Sneha. P		✓
23.	Suruthi, B		✓ ·
24.	Thamar Mohamed		√ ·
25.	Thasneem. MI		· /
26.	Vasimakaram. A		<i>y</i>
	Vineeth Kumar, R		
27.			
28.	Vishnupriyan. R	-	✓
29:	Vijay. K		
30.	Aabitha Begam. S	· · · · · ·	
31.	Abdul Ajeez. A	✓ -	
32.	Abdul Rahman. M	<b>✓</b>	
33.	Afsana. A	✓ .	
34.	Ahamed Aakif. Z		
35.	Akash. S		
	Akshaya. M	<b>✓</b>	
36.		<b>V</b>	
37.	Ammu. P	. 🗸	
38.			
39.	Annal Jebaseeli D	<b>√</b>	
40.	Antony Jero. J	<b>/</b>	
41.	Arthi. J	✓ ·	

SL. NO	STUDENT NAME	Hardware Modeling Using Verilog	CP2 Arduino based Embedded System Design
42.	Asrath Nisha. S	V	
43.	Boomika. P		<b>√</b> , ≡.'
44.	Chaandhini. C-	V	The state of the s
45.	Daniel Vinith. G	V -	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
46.	Defi Christina, C	V	
47.	Deiva Rani. M	<b>→</b>	
48.	Fazil Mohammed. B		
49.	-Gayathri, K		
50.	Harini. P		
51.	Hasiba Banu, H	V	
52.	Hina, M	✓ ·	
53.	Janani. M		
54.	Jansirani. K		
55.	Jasmine. E	· /	
56.	Karan. M		✓
57.	Kavitha. M		
58.	Kowsalya. K		
59.	Krishnapriya. K	_	
60.	Manikandan. T	<b>√</b>	
61.	Mathina Beevi. S	V	
62.	Mohamed Rizvanudeen, M		<b>√</b>
63.	Mohamed Suwaidee, M		✓
64.	Mohamed Ibrahim, M		✓ .

SL. NO	STUDENT NAME	CP1 Hardware Modeling Using Verilog	<u>CP2</u> Arduino based Embedded System Design
65.	Niranjani. B	1	
66.	Nithiksha. N		
67.	Nithish Kumar. S	<b>✓</b> .	ALC:
68.	Pavithra. C	V	
69.	Puvanithy. M	V	5
70.	Rizvana Begam. T	<b>√</b>	
71.	Sabarinath. C	<b>/</b>	
72,	Sabitha. S	<b>√</b>	
73.	Safa Almaz. MS	<b>✓</b>	
74.	Sathiya Sheela. S		
75.	Selciya. M		
76.	Shakthivel. A		<b>√</b>
77.	Shalini. B		<b>~</b>
78.	Suruthi. M		<b>*</b>
79.	Tamil Mani. B		
V93=33.0	Thajudeen. T		<b>√</b>
80.	Thilsara. S	-	<b>√</b>
81.	Vengatesh Kumar. M		
82.	Vigneshwaran, M		
83.	the state of the s		2
84.	Vimal Athithan. M		<b>√</b>
85.	Yogapriya. S	<b>✓</b>	
86.	Zam Zam Haliya. A	✓	
87.	Nisha Shalini. K	✓	

SL. NO	STUDENT NAME	EP1 Hardware Modeling Using Verilog	<u>CP2</u> Arduino based Embedded System Design
88.	Deepa. A		
89.	Hari Vijay. R		
90.	Kiruthigha. K		<b>V</b>
91.	Monica. J		<b>V</b>
92.	Vetriselvi, A		<b>√</b>
93.	Aarthi. N	_	3
94.	Abarna, N	<b>✓</b>	*
95.	Abdul Malik. T	V	
96.	Ameer Sultan, J	<b>✓</b>	
97	Ashik Mohamed. A	<b>-</b>	
98.	Asrin Jaswani. S		
99.	Bhuvaneswari, S	<b>√</b>	*
100.	Gayathri Vani. A		
101.	Guna Sunthari, B		
102.	Hari Haran. R		
103.	Lavanya, P	✓	
104.	Madhumitha. C	✓ ·	
105.	Mohamed Faisal. S	✓- n <sub>a</sub>	ARTON AND AND AND AND AND AND AND AND AND AN
106.	Mohamed Imran. M	2	7
107.	Mohamed Rafik. M		
108.	Mohamed Riaz. A		
109.	Mohamed Rizwan. B		~
110.	Mohamed Sirajudeen, S		



SL. NO	STUDENT NAME	CP1 Hardware Modeling Using Verilog	CP2 Arduino based Embedded System Design
111.	Muhammed Azarudeen. J		
112.	Muthulakshmi. M	V	1000
113.	Muthulakshmi, S		
114.	Pavithra Devi. P	V	— 1
115.	Pearly, J	V	
116.	Raeisa, A	_	
117.	Rifansiya. S	7.	
118.	Shabhan, R	<b>√</b>	
119.	Souban Mohamed. S		
120.	Suguna. S	<b>√</b>	
121.	Surendhar, B	Y	
	Syed Sadham. N		
122.	Thaslima Afrin, S	_	
123.		<b>√</b>	
124.	Vishnu Priya. N.J		
125.	Viveka. K	<b>√</b>	
126.	Fayaz Ahamed. A	<b>✓</b>	
127.	Haribaskar. S		
128.	Janani. R		
129.	Mohamed Ishan. M		
130.	Mohamed Rayan, A.S	y	
131.	Mohana Sundari, P		
132.	Vishnuvarthan, N	4	

HODECE

Pennight



(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai)
TRICHY – PUDUKKOTTAI ROAD, TIRUCHIRAPPALLI – 620 007.
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Website: - www.miet.edu

Ph: 0431 - 2660 303

### Certificate Program (III Year /V semester and IV Year/VII Semester)

Program Schedule

Name of the Course: Hardware Modeling Using Verilog

Course Code: EC19201

Course Coordinator: Mrs.N.Latha AP/ECE and Dr.A Suresh Kumar Ap/ECE

Total Hours: 36

Academic Year: 2019-2020

SI.No	Topics to be Covered	Hours	Date of Delivery
1.	Overview of Digital Design		
2.	Principles of combinational logic		
3.	Combinational circuit design		
4.	Combinational Functions		
5.	Analysis and design of combinational logic	- 8	23.05.19
6.	Sequential Logic Circuits-Latches	İ	*
7.	Flip-Flops		
8.	Counters and FSM design and their applications		
9.	Basic Concepts of Verilog		2
10.	modules and module instances		
11.	parts of a simulation, design block		
12.	Design block, stimulus block, trends in HDLs.		
13.	Basic Concepts- Verilog HDL	7	24.05.19
14.	Hierarchical Modeling Concepts-Top-down and bottom- up design methodology.		
15.	Language and conventions: Identifier, data types, Systematics, compiler directives.		
16.	Modeling using basic Verilog gate primitives		
17.	Description of and/or and buf /not type gates		
18.	Rise fall and turn-off delays,	7	27.05.10
19.	Min, Max, and Typical Delay and Instantiation	7	27.05.19
20.	DataflowModeling Continuous assignments		
21.	Delay specification, Expressions		

Sl.No	Topics to be Covered	Hours	Date of Delivery
22.	Operators, Operands, Operator Types		
23.	Behavioral modeling- Structured procedures		
24.	Initial and always, blocking		
25.	Non-blocking statements		
26.	Delay control, generate statement,	7	28.05.19
27.	Event control, conditional statements		20.03.19
28.	Multi way branching, loops,		- 172
29.	Sequential and Parallel blocks.		
30.	Application		
31.	Simulation of Combinational Circuits	-	
32.	Implementation of Combinational Circuits		
33.	Simulation of Sequential Circuits		
34.	Implementation of Sequential Circuits		
35.	Implementation Using FPGA		29.05.19
36.	DSP kernels on Xilinx/Altera boards		

H<sub>0</sub>D/ECE

Principal



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#### Resource Person Details

Title of the program	Hardware Modeling Using Verilog
Course Code	EC19201
Duration and timing of the program	36 Hrs, 09.30 AM – 05.00 PM
Name of the resource person	Mrs.N.Latha AP/ECE
Photo of the resource person	
Email address	Latha.n@miet.edu
Contact number	9629153633
Designation	Assistant Professor
Educational qualification	<ul> <li>B.E -Electronics and Communication Engineering 2006 in RMK College of Engineering (Anna University), Chennai, Tamil Nadu, with 82%.</li> <li>M.E -VLSI DESIGN (2010-2012july) in Oxford Engg College, affiliated to Anna University Chennai with CGPA 8.03.</li> </ul>
Experience	➤ Teaching Experience – 9 Years.



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Website: - www.miet.edu

Ph: 0431 - 2660 303

Title of the program	Hardware Modeling Using Verilog .
Course Code	EC19201
Duration and timing of the program	36 Hrs, 09.30 AM – 05.00 PM
Name of the resource person	Dr.A Suresh Kumar Ap/ECE
Photo of the resource person	
Email address	dr.sureshkumar@miet.edu
Contact number	9865248904
Designation	Assistant Professor
Educational qualification	<ul> <li>B.E -Electronics and Communication Engineering 1994 in Mookambigai College of Engineering with 67%.</li> <li>M.E - Communication System (2001-2003) in National Institute of Technology ,Tiruchirappalli with 65%</li> <li>Ph.D- (2007-2016) optical Sensor SSN College of Engineering with 75%</li> </ul>
Experience	> Teaching Experience 17 Years

## M.I.E.T ENGINEERING COLLEGE, TRICHY - 7. DEPARTMENT OF ELECTRONICS AND ELECTRONICS ENGINEERING

Value Added Courses (III/V Year - V /VII Semester)

#### Attendance Sheet

Name of the course: Hardware: modeling Using Ventog

Course Coordinator: Mrs.N.Latha., AP/ECE

Academic Year: 2019 - 2020

SL.NO	ROLL NO	STUDENT NAME	- 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1.	E1174001	Aabitha Begam. S	1	/	a	1	1	,	2	a	1	1	1	0	a	a	,	a	. ,	a	,	-
2.	E1174004	Abdul Ajeez. A	a	a	1	,	a	a	1	1	a	,	,	1	1	j	a		a	1	a	0
3.	E1174005	Abdul Rahman. M	1	1	a	a	1	1	1	a		,	Cu	_		,	a	/	7	,	1	1
4.	E1174013	Annal Jebaseeli. D	1	1.	1	,	1	1	a	1	a	,	1	a	a	a		a	a	1	1	1
5.	E1174014	Antony Jero. J	a	1	1	,	,	a	1	,	. 1	2	,	/	a	a	/	,	/	,	a	0
6.	E1174015	Arthi. J	1	à	1	1	a	1	1	a	_/_	,	,	,	,	a	,		1	1	a	
7.	E1174016	Asrath Nisha. S	1	1	a	1	/	1	1	a	1	,	,	1		a			1	1	a	1
8.	E1174019	Chaandhini. C	1	1	a	a	1		a	1	$\frac{1}{\alpha}$	,	0	1	,	1	0	/	1	,	,	0
9.	E1174020	Daniel Vinith. G	a	1	1		1	1	a	,	a	1	C	1	b-	a	,	a	1	,	a	,
10.	E1174026	Hasiba Banu, H	1	1	a	1	1	-/	1	1	a	,	a	7	1	a	/	a	,	,	a	1
11.	E1174027	Hina. M	/	1	1	1	a	a	1	a		a	1	1	,	1	,	a	a		1	1
12.	E1174029	Jansirani. K	1	a	1	a	1	1	1	1	,	a	1	<u>a</u>	1	1	,	a	· A	,	/	
13.	E1174030	Jasmine. E	1	1	1	/	1	/	1	G	/	a	1	1	1	,	1	a	/	1	a	0

SL.NO	ROLL NO	STUDENT NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
14.	E1174033	Kavitha. M	a	1	1	,	1	a	a	1	1	,	a	,	,	,	-	a	,	a	,	1	
15.	E1174034	Kowsalya. K	1	1	1	a	1	1	1	,	a	1	a	,	<del>/</del> ,	a	1	,	1	,	1	1	2
16.	E1174035	Krishnapriya. K	a	1	1	,	1	a	1	1	1	1	a	1.	1	1	,	/	/	<del> </del>	/	a	1
17.	E1174037	Manikandan. T	a	,	1	,	a	1	1	,	a			a	,	1	1	1	/	,	-/,	a	-
18.	E1174038	Mathina Beevi. S	1	a	a	<u>'</u> ,	1	1	1	,	1	/	a	1	_/_	1	1		1	/	<u>'</u>	Ce	-
19.	E1174043	Niranjani. B	1	1	1	a	1	a	,	,	1	,		,	,	/	a	-	<del>/</del>	a	1	/	1
20.	E1174044	Nithiksha. N		0	a	1	,	1	/	<i>'</i>	a	$\frac{1}{2}$	1,	_/_	1/	1	a	/	1	1	a	1	7
21.	E1174045	Nithish Kumar. S	a	1	1	a	a	1	1	,	$\alpha$	$\frac{a}{\prime}$	/	a	1	a	,	1	/	a.	/	a	
22.	E1174046	Pavithra. C	a	,	1	1	,	a	1	a	1	a	,	,		/	,	a	-	1	/		-
23.	E1174047	Puvanithy. M	1	\( \tag{\tau} \)	a	1	a	,	a	,	a	1	/,			1	,	,	,	/	/	1	-
24.	E1174049	Rizvana Begam. T	1	,	1	i	a	1	1	,	a	/	1,	a	1	a	,	<u>a</u>	/	/,		a	
25.	E1174050	Sabarinath. C	1	,	1	,	,	,	1	1	1	,	a	1	1,	$\frac{\alpha}{a}$	a_	d	a	1	a	/	
26.	E1174051	Sabitha. S	1	1	a	1	1	,	,	a	,	/	a	,	,	,		<u>/</u>				a	
27.	E1174052	Safa Almaz. MS	1	1	0	1	.,	1	,	1	1	a	1	a	<i>'</i> , '	,	/	a	a	1	/	1	
28.	E1174053	Sathiyaseela, S	/,	α	1	1	1	1	,	1	1	/	,	a	1	1	a	1	,	,	,	1	
29.	E1174054	Selciya. M	1	a	1	1	1	,	,	1	a	/	a	1	,	1	,	,	a	1	1	1	
30.	E1174055	Shakthivel. A	a	1	a	a	1	a	1	a	1	,	a	/	/	1	a	1	1	1	1	1	

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SL.NO	ROLL NO	STUDENT NAME	1 -	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
31.	E1174060	Thajudeen. T	1	1	1	a	a	1	1	1		a	,		,		0	١,	ļ.,	-1		,
32.	E1174061	Thilsara. S	a	a	,	,	1	a	1	1	,	0	a	1	1	0	10	1	/	10	a	/
33.	E1174063	Vigneshwaran. M	1	1	,	,	0	1	1	1		a	1	2	1	1,	0	1	1	a	,	-/
34.	E1174064	Vimal Athithan. M	/	1	,	a	1	a	1	1	a	1	a	1	,	1	1	1	-	,	,	1
35.	E1174066	Yogapriya. S		,	1	1	,	a	1	1	,	,	1	a	a	1	0	1	1	1	/_	a
36.	E1174067	Zam Zam Haliya. A	a	a	-/	1	1	1	a	1	,	a		0	,	a	1	,	a	a		
37.	E2184068	Nisha Shalini. K	1	1	a	,	1	a	1	,	a	01	1	,	-1	/	1	,	1	,	/	- /
38.	E1164001	Aarthi. N	a	a	a	a	1	1	a	,	1	1	a	,	,		a	/	1	/		/
39.	E1164002	Abarna. N	1	1	1	,	O	,	a	)	,	1	1	a	1	a	1	a	,		/	
40.	E1164005	Ashik Mohamed. A		1	1	,	1	,	1	a	a	a	7	01	1		,	a	a	2	a	a
41.	E1164006	Asrin Jaswani. S	a	a	1	1	1	1	a	1	1	/	a	1	,	/	a	,	1	-/	/	_/
42.	E1164007	Bhuvaneswari. S	1	1	,	a	,	,	,	,	,	,	1	-/	a	/_	a	/	1	/	/	1
43.	E1164009	Gayathri Vani. A	1	<u>/</u>	1	1	a	,	,	,	,	1	1	,	1	/		a	a	a	/	1
44.	E1164011	Guna Sunthari. B	æ	α	,	,	1	a	/	,	a	,	a	,	1	a	a	1	,	,	,	,.
45.	E1164014	Lavanya. P	1	1	1	,	1	,	a	1	,	1	a	1	/	1	a	,	1	,	,	1
46.	E1164015	Madhumitha. C	1	1	,	a	1	a	1	1	a	a	1	a	a	,	,	<i>'</i>	1	a	a	,
47.	E1164016	Mohamed Faisal. S	/	^	,	a	,	a	1	a		1	1	/	,	$\frac{1}{a}$	/	,	a	1	a	1

SL.NO	ROLL NO	STUDENT NAME	1	2	3	4	5	6	7	8	9	10	11	1,2	13	14	15	16	17	18	19	20
48.	E1164017	Mohamed Imran. M	a	1	1	a	1		a			a	a		a	a	a	a				
49.	E1164018	Mohamed Rafik, M	1	2	,	a	-	/	a	a	a	1	1	1	1	a	1	1	a	a	1-	0
50.	E1164019	Mohamed Riaz. A	1	1	1	1	1	1	1	a	1	1	1	1	-/ a		1	1	a	- 1	1	9
51.	E1164023	Muthulakshmi. M	a		1	1	a	1	1	2	1	1	1	1	1	1	1	,	1		a	1
52.	E1164024	Muthulakshmi. S	1	a	1	a	1	,	1	1	a	1	1	1	a	1	1	a	1	,	oc	1
53.	E1164025	Pavithra Devi. P	,	1	,	1	1	1	,	1	a	1	a	1	1	a	1	/	a	a	_/	a
54.	E1164026	Pearly. J	a	1	1	,	a	0-	,	a	1	1	1	a.	1	a	1	1	1	a	1	a
55.	E1164029	Racisa. A	. 1	a	1	a	1	1	1	a	/	1	1		a.	1	a	1	a		a	1
56.	E1164031	Rifansiya. S	1	1	1		a	1	,	a	1	/	1	1	a	a		a	1	1	1	1
57.	E1164032	Shabhan. R	1	1	1	1	1	a	,	1	a	a	a	1	/	,	1	1	1	,	,	1
58.	E1164033	Souban Mohamed. S	a	. /	1	1	1	/	1	1	a	1	1	a	1	1		,	a	/	,	1
59.	E1164034	Suguna. S	1	a	ca	1	1	1	1	1	. /	,	1	/	a	,	1	a	7	a	1	e.
60.	E1164037	Thaslima Afrin. S	1	1	1	1	a	1	a	1	1	1	1	1		a	1	/	a	1	a	/
61.	E1164040	Vishnu Priya. N.J	a	1	1	1	a	1	1	1	1	1	a	/	a	1	1	7	,	1	2	1
62.	E1164041	Viveka, K	a	1	1	,	a	-1	1	a	1	1		a	1	1	a	1	7	1	/	en
63.	E2174043	Fayaz Ahamed. A	1	1	1	1	1	a	,	ol.	1	,	a	/	1	1	a	9	/	a	1	9
64.	E2174044	Haribaskar. S	/	a	1	a	1	2	,	/	0-	a	1	on	0	1	a		a	A.	1	On

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SL.NO	ROLL NO	STUDENT NAME	1	2	.3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
		DI ODENT NAME	1	1	,	1	1	1	1	1	,	_	1	^		1		^	,	^		1
65.	E2174045	Janani. R	1	1	1	1	1	1	1		6	1	1	1	/-	1			-	-		,
66.	E2174046	Mohamed Ishan. M	1	1	1	1	1	1	1	<i>(</i> )	1	1	1	1	-	,	/	/	/	/		1
67.	E2174047	Mohamed Rayan, A.S	1	1	1	1	1	1	1	-	1	1	1	^	1	,	1	-	1	/		-
68.	E2174050	Vishnuvarthan. N	0	1.	1	1.	1	1	1	/	1	1	1	/	1	/	1	1	1	1	1	1
		Total No Students Presents													H		19					
		Total No Students Absent																				
		Signature Course Coordinator	Ju	J.	1	Le	-	6	1	1	L	129	Y	Se.	A.	J-1	Ruf	1		,	1	1
		15	1	1	1.		1			7	9	781	7	w.,	7-1	<u> </u>	X,	-	1	,	4	1

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Principal

# M.I.E.T ENGINEERING COLLEGE, TRICHY - 7. DEPARTMENT OF ELECTRONICS AND ELECTRONICS ENGINEERING

Value Added Courses (III/V Year - V/VII Semester)

Attendance Sheet

Name of the course: HIGH & WINTER OGO WING USER Course Code: EC19201

Course Coordinator: Mrs.N.Latha., AP/ECE

Academic Year: 2019 - 2020

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SL.NO	ROLL NO	STUDENT NAME	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	4(
1.	E1174001	Aabitha Begam. S	/	a	1	a	1	a	. ,	1	a	1	_	a	/	a	1	a	/		a	1
2.	E1174004	Abdul Ajcez. A	a	1	1	1	a	1	1	1	1	a	a	a	1	1	a	1	1	1	1	0
3.	E1174005	Abdul Rahman. M	1	a	1	1	4	1	a	/		1	1	1	a	1		,	1	Q	0-	1
4.	E1174013	Annal Jebaseeli. D	1	1	a	1	1	1	1	a	1	,	a	1	a	a	1	1	1	/	1	0
5.	E1174014	Antony Jero. J	1	1	1	1	1	/	1	2	a	1	1	a	1	1	a	1	a	1	a	
6.	E1174015	Arthi, J	1	1	1	,	a	,	1	1	1	Ci		a	,	11	/	1	-/	1	1	(
7.	E1174016	Asrath Nisha. S		a	1	1	1	1	1	1	1	1	a	,	a	a	1	1	1	1	,	0
8.	E1174019	Chaandhini. C	a	1	a	a	1	1	a	1	a	1	1	1	a	1	1		1	1	2	1
9.	E1174C20	Daniel Vinith. G	1	1	1	1	1	1	,	1	1	1	1	a	1	1	a	1	2	,	,	1
10.	E1174026	Hasiba Banu. H	1	1	1	1	1	1	,	,	1	,	a	1	1.	a	a	1	~	a	,	1
11.	E1174027	Hina. M	(	/	1	1	1	1	a	a	a	-/	1	1	1	1	1	1	1	1	a	/
12.	E1174C29	Jansirani. K	,	1	a	/	a	/	1	/	1	1	1	1	1	1	1	a	1	1	a	/

	,															IHH						
SL.NO	ROLL NO	STUDENT NAME	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
13.	E1174030	Jasmine, E	,	a	0	la	.0	-	,	1	a	,	a	,				,	-			
14.	E1174033	Kavitha. M	1	1	1	a	1	a	1	1	1	1		,	0	2	1	2	a	a	a	(
15.	E1174034	Kowsalya. K	1	1	0		1	1	,	1	/	a	_/_		a	a 1	a	1	1	2	/	
16.	E1174035	Krishnapriya. K	a	a	1	a	1	1	2	1	a	,		_/	a	1	1	1	1	1	1	
17.	E1174037	Manikandan. T	1	1	a		1	1	1	1	a	-	1	a	1	a	/	a	/	,	/	
18.	E1174038	Mathina Beevi. S	1	1	1	1	a	1	1	0	1	,	,	a	1	,	a	a	/	a	1	a
19.	E1174043	Niranjani. B	,	à	1	1	1	a	a	1	/	,	,	1	/	,	1	1	1	a	1	
20.	E1174044	Nithiksha. N	/	1	1	,	1	1	,	1	a	a	/	/	a		Ca	a	1	1	<del>,</del>	-/
21.	E1174045	Nithish Kumar. S	a	1	,	,	7	1	,	a	1	/	,	2	,	-	a	,	,	a	/	0
22.	E1174046	Pavithra. C	1	a	a	1	a	a	a	1	a	/	a	1	1	1	a	a	,	,	,	1
23.	E1174047	Puvanithy. M	1	1	,	1	0-	1	,	1	a	1	1	a	2	a	1	a	,	1	/	1
24.	E1174049	Rizvana Begam. T	1	1	1	1	1	1	,	1	/	1	1	/	ji.	a	1	/	Or	,	1	1
25.	E1174050	Sabarinath. C	a	1	a	/	1	a	1	1	1	1	,	/	7		/	00	1	1	1	1
26.	E1174051	Sabitha. S	a	1	a	/	1	a	1	1	1	1	a		1	a	/	a	/	a	1	-
27.	E1174052	Safa Almaz. MS	/	a	/	a		a.	/	1	a	1	a	1	1	1	/	a	a	/	1	1
28.	E1174053	Sathiyaseela. S	1	1	1	1	1	1	a	1	a	,	1	/	/	a	1	/	a	/	,	1
29.	E1174054	Selciya. M	1	1	1	,	/	1	a	,	1	1	a	a	a	1	1	0	1	/	/	6

SL.NO	ROLL NO	STUDENT NAME	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
30.	E1174055	Shakthivel. A	a	-1	1	1	a	_	1	1	,	a	,	0	0	,	1	,	a	-	1	-
31.	E1174060	Thajudeen. T	1	a	1	a	1	1	,	a	/	1	1	,	a	1	1	1		a	1	
32.	E1174061	Thilsara. S	a	1	a	1	a	a	1	1	a	1	a	1	1	,	0	/	,	1	1	a
33.	E1174063	Vigneshwaran. M	1	2	1	a	1	1	a	ne.	/	1	1	,	a	1	a	1	1	a	-	1
34.	E1174064	Vimal Athithan. M	1	1	0	1.	1	1	1	1	a	/	1	0		a	,	1	1	,		1
35.	E1174066	Yogapriya. S	1		1	a	1	/	1	a		-/	1	2	$\frac{2}{a}$	,	1	1	1	1 Q	1	0
36.	E1174067	Zam Zam Haliya. A	2	1,	a	1	a	a	,	1	a	1	,	,	a	1	/-	1	1	1	a	
37.	E2184068	Nisha Shalini. K	1	_/	1	a	7	1	/	1	a	/	/	1.	a	/	a	1	a	1	1	-
38.	E1164001	Aarthi. N		-/	1	a	.,	1	1	2	4	-	/		/	a	1	a		/	-	a
39.	E1164002	Abarna. N	- /	7	a	1	a	1	,	a	/	a	/	1	1	2	1	OL	1	a	,	1
40.	E1164005	Ashik Mohamed. A	a	0	OL	or	1	1	a	7	a	1	a	-/-	/		<i>(</i> .	7	,	,	1	1
41.	E1164006	Asrin Jaswani. S	1	/		a	1	1	4		2	-/	,	/	A	$\alpha$	_		/	1	/	a
42.	E1164007	Bhuvaneswari. S		/	1	a	1	1	1		a	/	01	/	/	a	,	$\frac{1}{a}$	/	a	1	a
43.	E1164009	Gayathri Vani. A		a	a	1	1	1	,	12	a	/	/	a	a	1	-	a	/	-		-
44.	E1164011	Guna Sunthari. B	a	1	1	a	1	1	/_	a		a	,	/	,	1		1	,	a	/	a
45.	E1164014	Lavanya. P	/	/	a	1	a	1	1	2		1	1	/	/	,	1	/	/	1	a	1
46.	E1164015	Madhumitha. C	/	/	1	a	1	/	/	1		,	1	1	2	a	1	/	/	/	/	,

	F		1				_		_	_							_	_	,		,	
SL.NO	ROLL NO	STUDENT NAME	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
47.	E1164016	Mohamed Faisal. S	1	1	1	1	1	a	ac	1	a	1	a	1	1	0	1	a	,	a	/	
48.	E1164017	Mohamed Imran. M	1	a	1	a	1	a	-	a	1	a	1	1	1	1	1	1	1	,	1	1
49.	E1164018	Mohamed Rafik. M	1	1	a	a	a	1	a	1	a	1	a	1	1	,	1	/	10		,	1
50.	E1164019	Mohamed Riaz. A	a	1	a		a	1	a	1	a	,	_	,	1	a	,	a	1	a	a	1
51.	E1164023	Muthulakshmi. M	1	3	1	a	a	1	1	a	1	a	1	1	0	1	a	1	a	a		0
52.	E1164024	Muthulakshmi. S	1	a	1	1	a	,	1	OL	1	a	1	,	1	,	1	a	1	1	,	/
53.	E1164025	Pavithra Devi. P	a	1	a	a	1	a	1	1	a	1	a	a	1	1	1	1	1	1	1	
54.	E1164026	Pearly. J	a	æ	1	1	,	,	1	1	/	a	./		a	1	a	1	1	,	1	1
55.	E1164029	Raeisa. A		1	a	1	a	1	1	/	a	1	1	,	a	a	1	4	,	,	,	1
56.	E1164031	Rifansiya. S	Q	1	a	a	1	a	/	1	,	2	,	7	,	a	1	1	,	,	1	7
57.	E1164032	Shabhan. R	1	1	a	/	1	1	a	a	a	1	a	a	a	1	00	'n	1	,	7	/
58.	E1164033	Souban Mohamed. S	a	a	/	/	a	1	1	,	2	a	1	1	1	a	-	a	1	1	1	-
59.	E1164034	Suguna. S	1	a	1	1	a,	1	a		oc	1	a	1	1	a	_a	,	a	1		1
60.	E1164037	Thaslima Afrin. S	1	1	1	a	1	a	1	a	a	/	cu/	7	a	a	1	a	/	/		1
61.	E1164040	Vishnu Priya. N.J	1	1	/	1	a	عر	a	1		a	/	a	1	/	,	1	a	a	9	/
62.	E1164041	Viveka, K	$\alpha$	1	1	a		a	1	a	a	a	1	a	a	1	a	$a_{l}$	Bi	-	7	
63.	E2174043	Fayaz Ahamed. A	/	a	1	1	1	a	a	1	a	/	a	a	1	a	1	,	,	a	1	4

			21	22	23	24	25	26	27	28	29	30	31	32	33	24	25	26	1.5	20		
SL.NO	ROLL NO	STUDENT NAME					-	20	21	20	29	30	31	32	33	34	35	36	37	38	39	40
64.	E2174044	Haribaskar. S	1	1		1	-	. ,	-	/	1	1			1		,		1			,
65.	E2174045	Janani. R	1	^	,	-	1	,	1	1	1.		,	/	/      ,	1	1	1	1	1	1	/
66.	E2174046	Mohamed Ishan, M	1	1	1	1	1	1	1	1	1	1	/	,	/	1	1	1	1	1	1	1
67.	E2174047	Mohamed Rayan. A.S	1	1	1	,	1	1	1	,	1	,	1	,	1.				1	1	7	1
68.	E2174050	Vishnuvarthan. N	1	1	1	1	1	1	1	,	1	1	(	,	1	1	1	_/	1	/	1	1
		<b>Total No Students Presents</b>	61	61	61	13	61	61	18	61	60	bo	60	60	60	65	15	65	65	65	65	65
		Total No Students Absent	٦	7	7	7	7	7	7	8	8	8	8	8	8	3	5	3	3	3	2	3
		Signature Course Coordinator	1	0			1	1	1		1	L	1			1	8	J.	0	1	Jan Jan	
		0	1	7	1	X	7	7-	7	4	4	7	5	5	1	1-			4	1	"	-0

HoD/ECE

Principal



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#### Certificate Program Assessment Test

Name of the course: Hardware Modeling Using Verilog Course Code: EC19201

Academic Year: 2019-2020

Date: 04.06.19 Time: 01:30 hrs

1. Which level of abstraction level is available in Verilog but not in VHDL?

- A. Behavioral level
- B. Dataflow level
- C. Gate level
- D. Switch level
- 2. Which logic level is not supported by verilog?
  - A. U
  - B. X
  - C. Z
  - D. None of the above
- 3. If a net has no driver, it gets the value
  - A. 0
  - B. X
  - C. Z
  - D. U
- 4. Default value of reg is
  - A. 0
  - B. X
  - C. Z
  - D. U
- 5. The task \$stop is provided to
  - A. End simulation
  - B. Suspend simulation
  - C. Exit simulator
  - D. None of the above
- 6. Externally, a output port must always connected to a
  - A. net only
  - B. a reg only
  - C. either net or reg
  - D. None of the above
- 7. If A=4'b011 and B=4b'0011, then the result of  $A^{**}B$  will be
  - A. 6
  - B. 9
  - C. 27
  - D. Invalid expression

	hal value of a=1 and b=2, then what will be final value		
	always @ (posedge clock)		
	a=b;		
	always @ (posedge clock)		
	b=a;		
	. a= 2, b=1		
	. a= 1, b=2		
C	. Both a and b will have same value either 0 or 1		
D	. None of the above		
9. At	ask can have arguments of type		
A	. Input only		
В.	Output only		
C.	Both input and output		
D.	. All input, output and inout		
10. Ini	tial value of a=1 and b=2, then what will be final val	ue if	
	always @ (posedge clock)		
	a<=b;		
	always @ (posedge clock)		
•	b<=a;	*	
A.	a= 2, b=1		
	a=1, b=2		
	Both a and b will have same value either 0 or 1	(4)	
D	None of the above		
10.			
	ven the following Verilog code, what value of "a" is o	displayed?	141
	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1;	displayed?	
	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a);	displayed?	
11. Giv	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end	displayed?	
11. Giv	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a);	displayed?	
11. Giv A. B.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0	1	
11. Giv A. B.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im	1	
11. Giv A. B.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im	1	
A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above	plementation	
A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above	plementation	ts in sensitivity list?
A. B. C. D. 12. In A.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting the state of the above.	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes  It depends on the coding style	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes It depends on the coding style None of these	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes It depends on the coding style None of these  w many flops will be synthesized by the given code?	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menti No Yes It depends on the coding style None of these w many flops will be synthesized by the given code? always @ (posedge clock) begin	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menti No Yes It depends on the coding style None of these w many flops will be synthesized by the given code? always @ (posedge clock) begin Q1<=d;	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menti No Yes It depends on the coding style None of these w many flops will be synthesized by the given code? always @ (posedge clock) begin Q1<=d; Q2<=q1;	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes It depends on the coding style None of these  w many flops will be synthesized by the given code? always @ (posedge clock) begin Q1<=d; Q2<=q1; Q3<=q2;	plementation	ts in sensitivity list?
A. B. C. D.  12. In A. B. C. D.	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes It depends on the coding style None of these  w many flops will be synthesized by the given code? always @ (posedge clock) begin Q1<=d; Q2<=q1; Q3<=q2; end	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D. 13. Hov	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes It depends on the coding style None of these  w many flops will be synthesized by the given code? always @ (posedge clock) begin Q1<=d; Q2<=q1; Q3<=q2; end 1	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D. 13. Hov	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes It depends on the coding style None of these  w many flops will be synthesized by the given code? always @ (posedge clock) begin Q1<=d; Q2<=q1; Q3<=q2; end 1 2	plementation	ts in sensitivity list?
A. B. C. D. 12. In A. B. C. D. 13. Hov	ven the following Verilog code, what value of "a" is a always @ (clock) begin a = 0; a <= 1; \$display(a); end 0 1 either 0 or 1 depending on depending on simulator im None of the above a pure combinational circuit is it necessary to menting No Yes It depends on the coding style None of these  w many flops will be synthesized by the given code? always @ (posedge clock) begin Q1<=d; Q2<=q1; Q3<=q2; end 1	plementation	ts in sensitivity list?

A. lns/lps B. 10ns/lps C. 100ns/100ps D. 100ns/110ps	- 2γ - 3γ
<ul> <li>15. If a recursive function is called concurrently from two locations, then</li> <li>A. Recursive function can have multiple calls concurrently</li> <li>B. It will result give ambiguous results</li> <li>C. It will result in an error</li> <li>D. Simulation will hang up</li> </ul>	
16. Which operators has highest precedence in verilog  A. Unary  B. Multiplication  C. Addition	
D. Conditional  17. Variable and signal which will be updated first?  A. Variable  B. Signal  C. Can't say	
D. None of the above  18. The output of an AND gate with three inputs, A, B, and C, is HIGH when	<u>.</u>
19.If a signal passing through a gate is inhibited by sending a LOW into one of the in HIGH, the gate is an: A.AND B.NAND C.NOR D.OR	puts, and the output is
20.A device used to display one or more digital signals so that they can be compared a diagrams for the signals is a:  A.DMM  B.spectrum analyzer  C.logic analyzer  D.frequency counter	to expected timing
21. When used with an IC, what does the term "QUAD" indicate? A.2 circuits B.4 circuits C.6 circuits D.8 circuits	
22. The output of an OR gate with three inputs, A, B, and C, is LOW when $\_$ A.A = 0, B = 0, C = 0 B.A = 0, B = 0, C = 1 C.A = 0, B = 1, C = 1 D.all of the above	
23. Which of the following logical operations is represented by the + sign in Boolean a	lgebra?

			* 1
A.inversion			
B.AND			
C.OR			
D.complementation			
24.Output will be a LOW for any case v	when one or more innu	its are zero for a(n).	
A.OR gate	men one or more inpo	its are zero for a(ii).	
B.NOT gate			
C.AND gate			The second second
D.NOR gate		the second of	
Service Control of the Control of th			
25. The format used to present the logic	output for the various	combinations of leads leaves	4
a(n):	output for the various	combinations of logic inputs	to a gate is called
A.Boolean constant			
B.Boolean variable			
C.truth table			
D.input logic function			
1 3			
26. The power dissipation, PD, of a logic	gate is the product of	dt a	
A.dc supply voltage and the peak current	gate is the product of	tne	
B.dc supply voltage and the average suppl	i) ourrant		
C.ac supply voltage and the peak current	y current		
D.ac supply voltage and the average suppl	v current		
and the average suppr	y current		
27. The Boolean expression for a 3-input	AND make to		
A.X = AB	AND gate is	_•	
B.X = ABC			
C.X = A + B + C			
D.X = AB + C			
D.A - AB + C		40.	
20 What does the small L. LLL			
28. What does the small bubble on the ou	itput of the NAND gat	e logic symbol mean?	
A.open collector output B.tristate			
			2
C.The output is inverted.  D.none of the above			2
D.none of the above			
20.1541			
29.If the output of a three-input AND ga	ate must be a logic LO	W, what must the condition of	of the inputs be?
A.All inputs must be LOW.			
B.All inputs must be HIGH.			
C.At least one input must be LOW.			
D.At least one input must be HIGH.			
30.Logically, the output of a NOR gate w	ould have the same B	oolean expression as a(n):	
A.NAND gate immediately followed by an	inverter		
B.OR gate immediately followed by an inv	erter		
C.AND gate immediately followed by an ir	iverter		
D.NOR gate immediately followed by an ir	iverter		
× =	20		
	1/		
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4	NV		2
Course Coordinator.	HoD/ECE		Principal
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(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai)
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#### Report

Name of the course: Hardware Modeling Using Verilog

Course Code: EC19201

Course Coordinator: Mrs.N.Latha AP/ECE and Dr.A Suresh Kumar Ap/ECE

Total Hours: 36 Academic Year: 2019-2020

I hereby affirm that the entire course contents listed in the course syllabus of the certificate program "Hardware Modeling Using Verilog" have educated to the students as the part of the prescribed co – curricular activities through Certificate Program.

They have been given hands on session on the topics mentioned and students clearly understood the verilog hardware description Language. It will help them to learn various digital circuits modeling issues using Verilog, Writing test benches.

I confirmed that the certificate program titled as "Hardware Modeling Using Verilog" has been conducted in the beginning of the semester and course delivery along with attendance of the students was recorded.

I confirmed that all the students were actively attended this certificate Program and performed well throughout the program and eligible students received the certificate.

Course Coordinator

HoD/ECE

Principal

M.I.E.T. ENGINEERING COLLEGE  Trichy, Pudukkottai Road, Trichy - 620 007.  Course Completion Certificate  INSTITUTIONS Since 1984
This is to Certify that Mr/Ms. A. Payaz Ahamed
of Wes has Completed the Course on
Hardweine Modeling Ving Venilog from 22.5.2019 to 30.5.2019
Course Coordinator And Aug Problem Principal
M.I.E.T. ENGINEERING COLLEGE GUNDUR, TIRUCHIRAPPALLI-620 007.

(33)	
	M.I.E.T. ENGINEERING COLLEGE Trichy, Pudukkottai Road, Trichy - 620 007.
	Course Completion Certificate INSTITUTIONS Since 1984
	This is to Certify that Mr/Ms. <u>H. kavitha</u> of <u>till ELE</u> has Completed the Course on
	Hardware Musteling Uning miles from 23.5.2019 to 30.5.2019
	Course Coordinator And Principal Principal
	M.I.E.T. ENGINEERING COLLEGE GUNDUR, TIRUCHIRAPPALLI-620 007.